



DESCRIPTION

The WM8816 is a highly linear stereo volume control for audio systems. The design is based on resistor chains with external op-amps, which provides flexibility for the supply voltage, signal swing, noise floor and cost optimisation. The gain of each channel can be independently programmed from -111.5dB to +15.5dB through a digital serial control interface.

Audible clicks on gain changes are eliminated by changing gains only when a zero crossing has been detected in the signal. The device also features peak level detection, which can be used for Automatic Gain Control. The WM8816 operates from a single +5V supply and accepts signal input levels up to ±18V.

The WM8816 is available in a 16-pin SOIC package. It is guaranteed over a temperature range of -40° to 85°C.

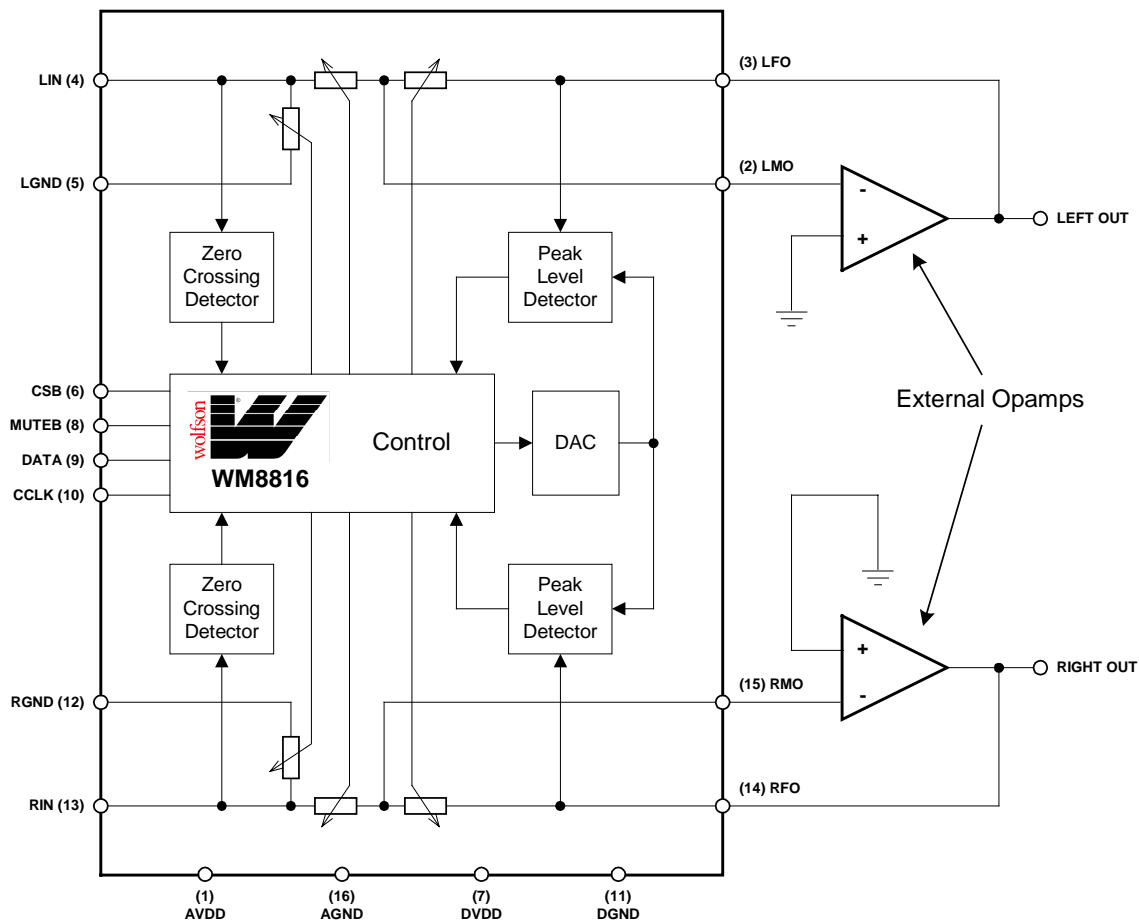
FEATURES

- Gain range from -111.5dB to +15.5dB
- 0.5dB Gain step size
- Total Harmonic Distortion 0.001% (100dB) typical
- Crosstalk -110dB typical
- Input signals up to ±18V
- Zero Detection for Gain Changes
- Hardware and Software Mute
- Power On/Off Transient Suppression

APPLICATIONS

- Audio Amplifiers
- Consumer Audio / Entertainment Systems
- Mixing Desks
- Audio Recording Equipment

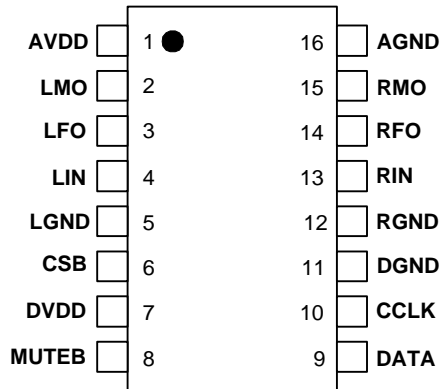
BLOCK DIAGRAM



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Advanced information data sheets contain preliminary data on new products in the pre-production phase of development. Supplementary data will be published at a later date.

## PIN CONFIGURATION



## ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM8816EDW	-40 to +85°C	16-pin SOIC (plastic)

## PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AVDD	Supply	Supply Voltage for Analogue Circuitry
2	LMO	Analogue Output	External Op-amp Inverting Input (Left Channel)
3	LFO	Analogue Input	External Op-amp Feedback Signal (Left Channel)
4	LIN	Analogue Input	Input Signal (Left Channel)
5	LGND	Analogue Input	Input Signal Ground (Left Channel)
6	CSB	Digital Input	Chip Select (active low)
7	DVDD	Supply	Supply Voltage for Digital Circuitry
8	MUTE B	Digital Input	Mute (active low)
9	DATA	Digital In / Out	Serial Interface Data Input / Output (tri-state)
10	CCLK	Digital Input	Serial Interface Clock
11	DGND	Supply	Digital Ground
12	RGND	Analogue Input	Input Signal Ground (Right Channel)
13	RIN	Analogue Input	Input Signal (Right Channel)
14	RFO	Analogue Input	External Op-amp Feedback Signal (Right Channel)
15	RMO	Analogue Output	External Op-amp Inverting Input (Right Channel)
16	AGND	Supply	Analogue Ground

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore susceptible to damage from excessive static voltages. To optimise the distortion and noise performance of pins 3, 4, 13 and 14, the on-chip ESD protection circuitry has been restricted, and consequently only achieves 300V when characterised to the Human Body Model. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specification JESD22-A112-A, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 3 and is therefore supplied in vacuum-sealed moisture barrier bags.

CONDITION	MIN	MAX
Input signal voltage	-20V	+20V
Positive supply voltage (AVDD to AGND, DVDD to DGND)	-0.5V	6V
Input voltage (all other pins)	-0.5V	AVDD + 0.5V
Operating temperature	-40°C	85°C
Storage temperature	-55°C	125°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal voltage			-18		+18	V
Positive supply voltage	AVDD, DVDD		4.5	5	5.5	V
Negative supply voltage	AGND, DGND			0		V
Input signal grounds	LGND, RGND			0		V
Operating temperature			-20	60	60	°C

## ELECTRICAL CHARACTERISTICS

### TEST CONDITIONS

AVDD = 5.0V, AGND = 0V, T<sub>A</sub> = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Inputs / Outputs</b>						
Input resistance	R <sub>IN</sub>	For any gain	7	10		kΩ
Input capacitance	C <sub>IN</sub>	For any gain		2		pF
Input offset voltage	V <sub>offset</sub>	External OP275 opamp, gain = 1			1	mV
Supply current	I <sub>DD</sub>	From AVDD / AGND		2.5	5	mA
Power supply rejection ratio (Note 1)	PSRR	From AVDD		80		dB
<b>Gain Control</b>						
Gain range	G		-111.5		+15.5	dB
Gain step size	D			0.5		dB
Gain error (Note 1)	DE	Lowest gains guaranteed by design, not tested in production.			0.5	dB
Gain match error (Note 1)	ME	Between channels			0.2	dB
Mute attenuation	MATT		113			dB

**TEST CONDITIONS**AVDD = 5.0V, AGND = 0V, T<sub>A</sub> = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Audio Performance</b>						
Noise (Note 1) V <sub>IN</sub> = 0V, V <sub>OUT</sub> with OP275, A-weighted	N	Gain = 0dB			13	μV rms
		Gain = -60dB		4		
		Gain = mute		2.5		
Total Harmonic Distortion plus Noise	THD+N	V <sub>IN</sub> = 1Vrms, gain=0dB, V <sub>OUT</sub> with OP275, DC to 20 kHz		0.001 (100)		% (dB)
Dynamic Range (Note 1)	DR		120	130		dB
Crosstalk (Note 1)	CR	Between channels, gain=0dB, f <sub>IN</sub> =1kHz	-100	-110		dB
<b>Digital Inputs / Outputs</b>						
Input low voltage	V <sub>IL</sub>	All digital inputs			0.3 DVDD	V
Input high voltage	V <sub>IH</sub>	All digital inputs	0.7 DVDD			V
Output low voltage	V <sub>OL</sub>	I <sub>Load</sub> = 2mA			0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>Load</sub> = 2mA	DVDD -0.4			V
<b>Control Interface Timing</b>						
Clock Frequency	f <sub>CCLK</sub>				1	MHz
Period of CCLK high	t <sub>WHC</sub>	V <sub>IH</sub> to V <sub>IH</sub>	500			ns
Period of CCLK low	t <sub>WLC</sub>	V <sub>IL</sub> to V <sub>IL</sub>	500			ns
Rise time of CCLK	t <sub>RC</sub>	V <sub>IL</sub> to V <sub>IH</sub>			100	ns
Fall time of CCLK	t <sub>FC</sub>	V <sub>IH</sub> to V <sub>IL</sub>			100	ns
Hold time, CCLK high to CSB low	t <sub>HCHS</sub>		20			ns
Setup time, CSB low to CCLK high	t <sub>SSLCH</sub>		100			ns
Setup time, valid DATA to CCLK high	t <sub>SDCH</sub>		100			ns
Hold time, CCLK high to invalid DATA	t <sub>HCHD</sub>		100			ns
Setup time, CCLK low to valid DATA	t <sub>DCLD</sub>	Load = 100pF			200	ns
Hold time, CSB high or 16 <sup>th</sup> CCLK low to invalid DATA	t <sub>DSZ</sub>	Load = 3.3kΩ	20		200	ns
Hold time, 16 <sup>th</sup> CCLK high to CSB high	t <sub>HLCHS</sub>		200			ns
Setup time, CSB high to CCLK high	t <sub>SSHCH</sub>		200			ns

**Note:**

1. Guaranteed by design.

### CONTROL INTERFACE TIMING DIAGRAM

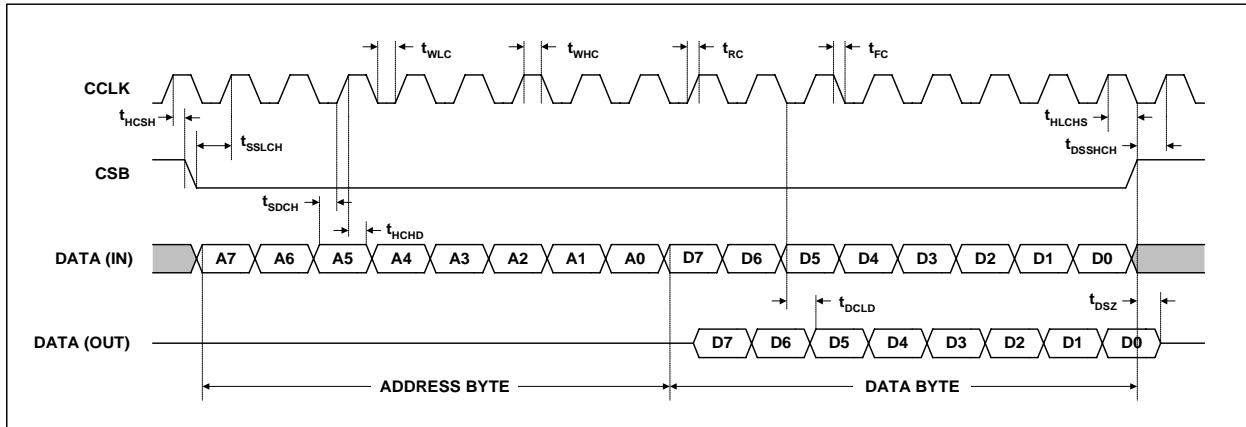


Figure 1 Control Interface Timing Diagram

## DEVICE DESCRIPTION

The WM8816 is a stereo digital volume control designed for audio systems. The levels of the left and right analogue channels can be programmed independently through the serial interface. The resistor values in the internal resistor chains are decoded to 0.5 dB resolution with multiplexers, giving a gain range of -111.5 to +15.5 dB. The code for -112 dB activates mute for maximum attenuation.

The WM8816 has two constant impedance signal inputs. The left channel input is between LIN and LGND, and the right channel between RIN and RGND. The output pins LFO, LMO (left) and RFO, RMO (right) are designed to interface directly to two external op-amps, which produce the volume controlled output signals. This provides flexibility for the supply voltage and signal swing; while the WM8816 runs at 5V, the output signal swing depends solely on the op-amp supply.

### INTERFACES

Control information is written into or read back from the internal register via the serial control port. This port consists of a bi-directional data pin (DATA), an active low chip select pin (CSB) and the control clock (CCLK). Control data is shifted into the serial input register on the rising edges of CCLK pulses, while CSB is low. All control instructions require two bytes of data. The first byte contains a 4-bit register address and a read/write bit, and the second byte is the control word. CSB must return to high at the end of each word. When reading from the control registers, data is shifted out on the falling edges of CCLK.

When CSB is high, the DATA pin is in a high impedance state. In a multi-channel system, the same DATA and CCLK lines can thus be connected to several WM8816 volume controllers, and each device can be independently addressed by pulling its CSB pin low.

### OPERATING MODES

When power is first applied, a power-on reset initialises the control registers mutes the WM8816. To activate the device, the MUTE pin must be high and a non-zero value must be written to the gain register. After that the device can be muted again either by pulling the MUTE pin low or by writing zero (00hex) to the gain register.

For device testing, the MUTE pin becomes an output when Bit 1 of the test register is high. Internal signals can then be directed to MUTE and monitored.

### CHANGING THE GAIN OF THE CHANNEL

The WM8816 has two gain registers for the left and right channels respectively. There is also an alias register address to update both gain registers simultaneously. When a new gain value is written into a gain register the WM8816 will wait until the next falling edge zero crossing in the input signal before changing the gain. This ensures that no audible click is produced at the output. If there are no zero crossings in the signal after 18ms, the gain is changed regardless. If both gain registers are changed simultaneously, the gain is changed first on the right and then the left channel.

### PEAK LEVEL DETECTION

The WM8816 has an on-chip 8-bit digital-to-analogue converter (DAC) used for monitoring the peak level of the output signal. The DAC input value is programmed via the serial interface. The reference value  $V_{REF}$  is calculated from  $V_{REF} = k/256 \times 18V$ , where  $k$  is the DAC input code. When a positive peak signal level exceeds this value, the peak detector sets Bit 1 (for the left channel) or Bit 0 (right channel) of the status register. These bits remain set until the status register is read.

## REGISTER MAP

REGISTER	ADDRESS BYTE BITS								DATA BYTE	
	7	6	5	4	3	2	1	0	MSB...LSB	Function
Peak Detector Status CR4	X	1	0	1	1	R/W	X	X	Output code 00000000 00000001 00000010 00000011	No overload Right overload Left overload Both overload
Peak Detector Reference CR3	X	1	1	0	0	R/W	X	X	Input code 11111111 11111110 11111101 : 00000010 00000001 00000000	DAC output 255/256 × 18V 254/256 × 18V 253/256 × 18V : 2/256 × 18V 1/256 × 18V AGND
Left Channel Gain CR2	X	1	1	0	1	R/W	X	X	Input code 11111111 11111110 11111101 : 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 : 0.0 -111.0 -111.5 mute
Right Channel Gain CR1	X	1	1	1	0	R/W	X	X	Input code 11111111 11111110 11111101 : 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 : 0.0 -111.0 -111.5 mute
Test, CR5	X	1	1	1	1	R/W	X	X	Reserved	
Both Channel Gains	X	1	0	0	1	W	X	X	Write to both gain registers	

Table 1 Register Map Description

## Notes:

- Address bit 2 is the read / write bit (1 for read, 0 for write).
- X are don't cares, set to 1 for minimum power consumption.
- All registers are set to their default value (all zeros) during power-on reset, except CR3 which is set to 255.

**TEST REGISTER**

When bit 1 in register CR5 is set, MUTE<sub>B</sub> becomes an output pin. Bits 2, 3 and 4 select different internal signals which can then be seen via the MUTE<sub>B</sub> pin.

CONDITION	DATA BYTE BITS								FUNCTION
	7	6	5	4	3	2	1	0	
Normal (MUTE <sub>B</sub> configured as input)	0	0	0	0	0	0	0	1	Latch the new gain value to resistor network
Test Mode  (MUTE <sub>B</sub> configured as output)	0	0	0	0	0	0	1	0	Left delay generator
	0	0	0	0	0	1	1	0	Left peak detector
	0	0	0	0	1	0	1	0	Left zero crossing
	0	0	0	0	1	1	1	0	Left enable for zero crossing and delay generator
	0	0	0	1	0	0	1	0	Right delay generator
	0	0	0	1	0	1	1	0	Right peak detector
	0	0	0	1	1	0	1	0	Right zero crossing
	0	0	0	1	1	1	1	0	Right enable for zero crossing and delay generator

Table 2 Test Register Description

**PERFORMANCE GRAPHS**

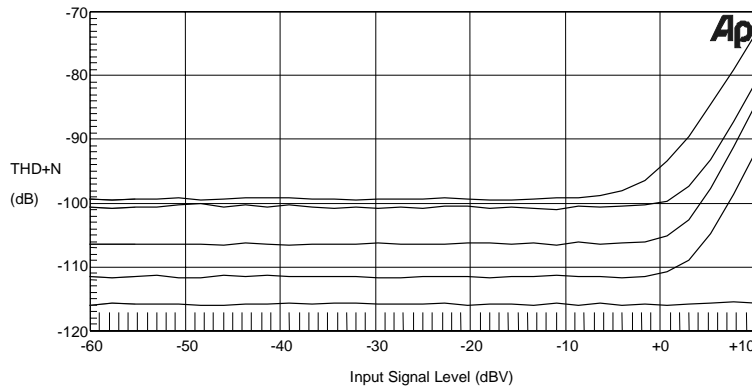


Figure 2 THD + Noise versus input level at gains of +6dB, 0dB, -6dB, -12dB and mute

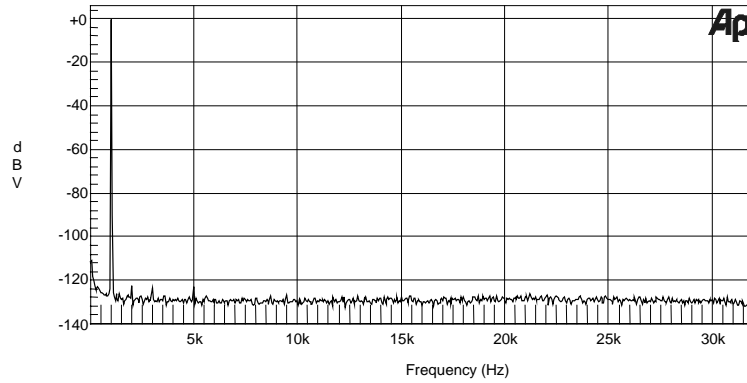
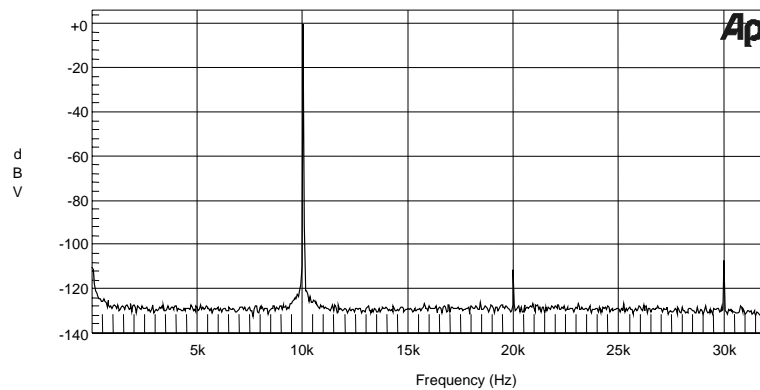


Figure 3 FFT of output signal with 1kHz, 1V rms sine wave input





**Figure 4** FFT of output signal with 10kHz, 1V rms sine wave input

#### **POWER SUPPLY DECOUPLING**

For best audio performance, all digital activities should be avoided during analogue signal processing. Special attention should be paid to power and ground decoupling. If possible separate analogue and digital power supplies should be used. A clean analogue power supply should be used for AVDD. DVDD should be the same as AVDD to avoid latch-up phenomena. Decoupling capacitors should be located as close to the WM8816 as possible.

RECOMMENDED EXTERNAL COMPONENTS

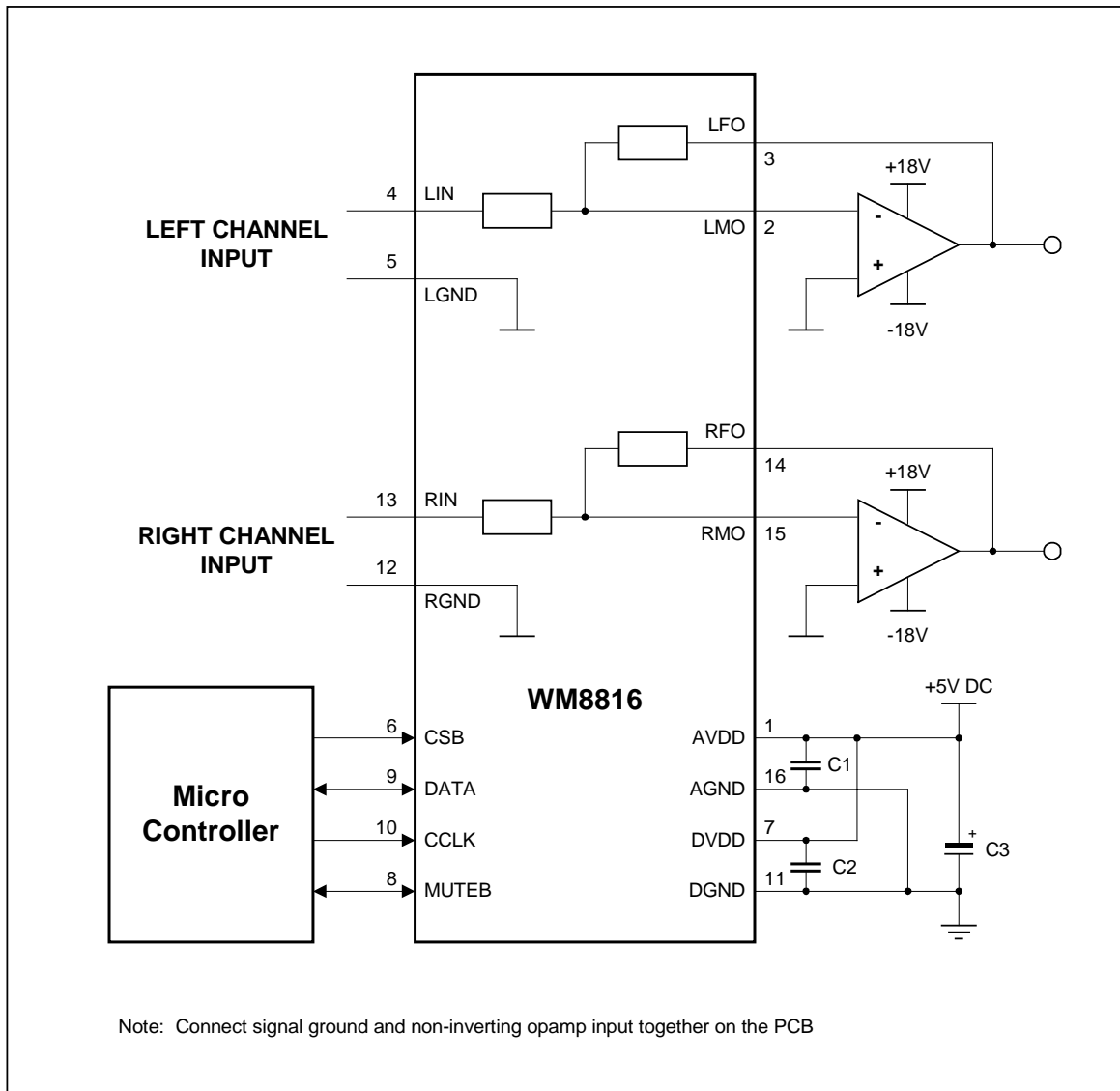


Figure 5 Typical Application

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	220nF	Analogue Supply Decoupling
C2	220nF	Digital Supply Decoupling
C3	10µF	General Supply Decoupling

Table 3 Recommended External Components Values

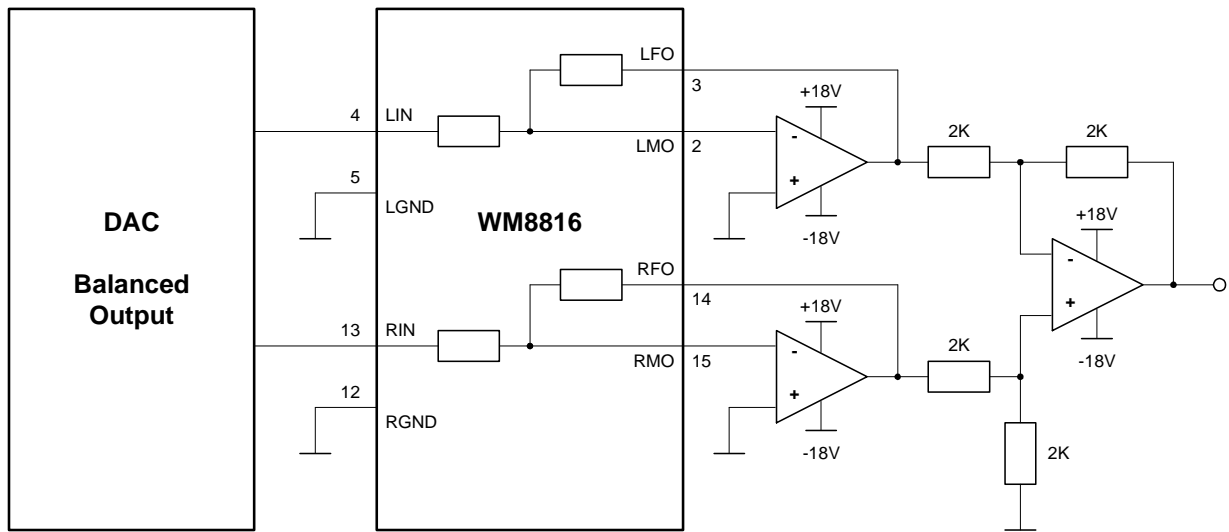
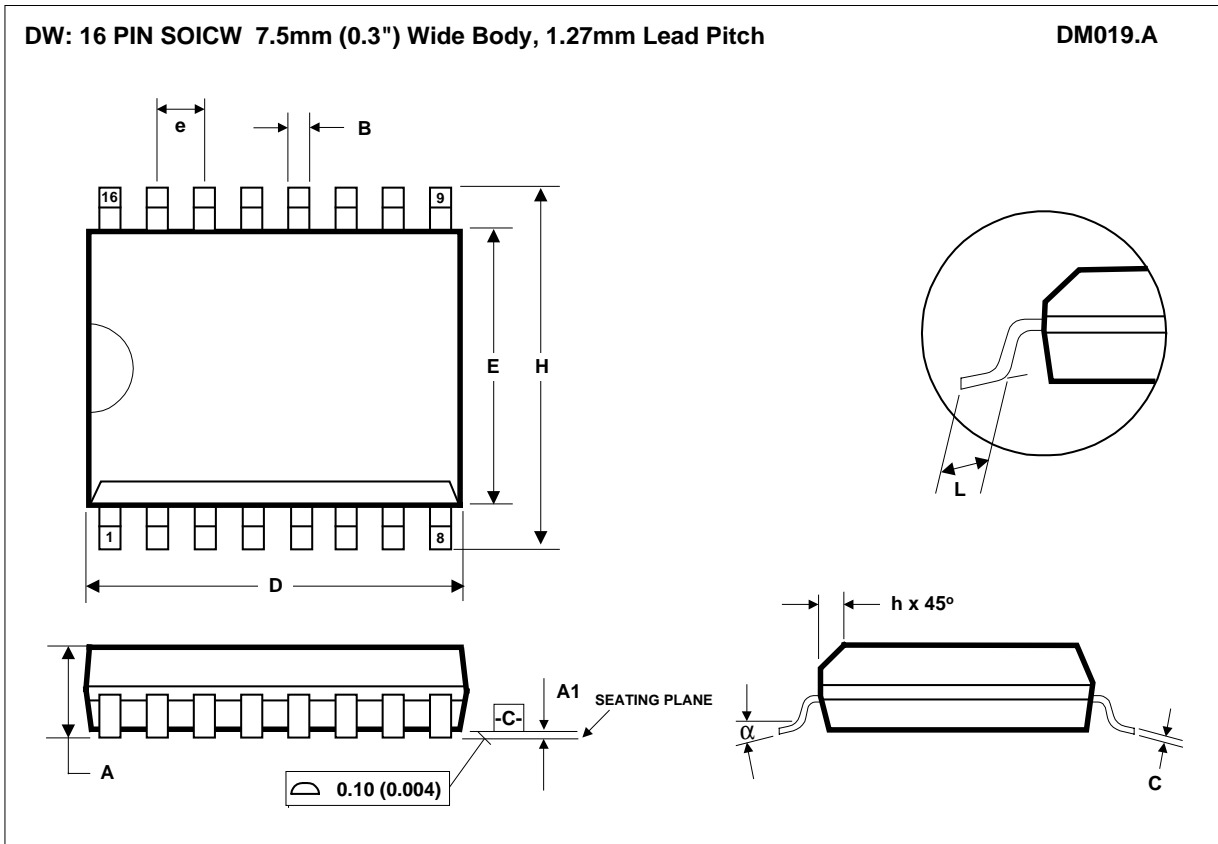


Figure 6 Configuration for Double Balanced Output (One Channel)

PACKAGE DIMENSIONS



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
<b>A</b>	2.35	2.65	0.0926	0.1043
<b>A<sub>1</sub></b>	0.10	0.30	0.0040	0.0118
<b>B</b>	0.33	0.51	0.0130	0.0200
<b>C</b>	0.23	0.32	0.0091	0.0125
<b>D</b>	10.10	10.50	0.3465	0.3622
<b>e</b>	1.27 BSC		0.0500 BSC	
<b>E</b>	7.40	7.60	0.2914	0.2992
<b>h</b>	0.25	0.75	0.0100	0.0290
<b>H</b>	10.00	10.65	0.3940	0.4190
<b>L</b>	0.40	1.27	0.0160	0.0500
<b>α</b>	0°	8°	0°	8°
<b>REF:</b>	JEDEC.95, MS-013			

NOTES:  
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).  
 D. MEETS JEDEC.95 MS-013, VARIATION = AA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.