HT93LC46

CMOS 1K-Bit Serial EEPROM

Features

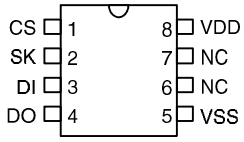
- Wide operating voltage range
  - Write:2.4~5.5V
  - Read: 2.0~5.5V
- Low power consumption
  - Operating: 5mA max.
  - Standby: 2μA max.
- Write cycle time <5ms
- Write operation with built-in timer
- Automatic erase-before-write operation
- Word/chip erase and write operation
- Auto-increment read operation
- Programming Status Indicator
- Software and hardware controlled write protection
- 10-year data retention after 100K rewrite cycles
- 10^6 rewrite cycles per word
- Operating temperature range: –40°C~+85°C
- 8-pin DIP/SOP package

General Description

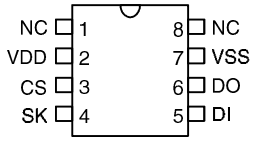
The HT93LC46 is a 1K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 1024 bits of memory are organized into 64 words and each word is 16 bits.

By popular microcontroller, the versatile serial interface including chip select (CS), serial clock (SK), data input (DI) and data output (DO) can be easily controlled.

Pin Assignment

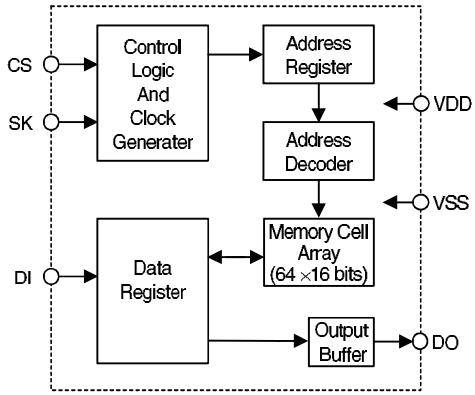


HT93LC46
– 8 DIP/SOP-A



HT93LC46
– 8 SOP-B

Block Diagram



Pin Description

Pin No.		Pin Name	I/O	Description
–A	–B			
1	3	CS	I	Chip select input
2	4	SK	I	Serial clock input
3	5	DI	I	Serial data input
4	6	DO	O	Serial data output
5	7	VSS	I	Negative power supply
6,7	8,1	NC	—	No connection
8	2	VDD	I	Positive power supply

Absolute Maximum Ratings*

Supply Voltage .....–0.3V to 6.0V
Storage Temperature.....–50°C to 125°C
Input Voltage.....V_{SS}–0.3 to V_{DD}+0.3
Operating Temperature.....–40°C to 85°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(Ta=–40°C to 85°C)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
		V_{DD}	Conditions			
V_{DD}	Operating Voltage	—	Read	2	5.5	V
		—	Write	2.4	5.5	V
I_{DD1}	Operating Current (TTL Input Level)	5V	DO unload, SK=1MHz	—	5	mA
I_{DD2}	Operating Current (CMOS Input Level)	5V	DO unload, SK=1MHz	—	5	mA
		2~5.5V	DO unload, SK=250kHz	—	5	mA
I_{STB}	Standby Current	5V	CS=SK=DI=0V	—	2	μA
I_{LI}	Input Leakage Current	5V	$V_{IN}=V_{DD}$~V_{SS}	0	1	μA
I_{LO}	Output Leakage Current	5V	$V_{OUT}=V_{DD}$~V_{SS} CS=0V	0	1	μA
V_{IL}	Low Level Input Voltage	5V	—	0	0.8	V
		2~5.5V	—	0	$0.1V_{DD}$	V
V_{IH}	High Level Input Voltage	5V	—	2	V_{DD}	V
		2~5.5V	—	$0.9V_{DD}$	V_{DD}	V
V_{OL}	Low Level Output Voltage	5V	I_{OL}=2.1mA	—	0.4	V
		2~5.5V	I_{OL}=10μA	—	0.2	V
V_{OH}	High Level Output Voltage	5V	I_{OH}=–400μA	2.4	—	V
		2~5.5V	I_{OH}=–10μA	V_{DD}–0.2	—	V
T_{RW}	Rewriting Times	5V	25°C V_{DD}=5V Block mode (Note 2)	10^6	—	Times/ word
C_{IN}	Input Capacitance (see Note 1)	—	f=250kHz	—	5	pF
C_{OUT}	Output Capacitance (see Note 1)	—	f=250kHz	—	5	pF

Note1: These parameters are periodically sampled but not 100% tested

Note2: The block mode exercises all the cells of the array simultaneously

A.C. Characteristics

(Ta=−40°C to 85°C)

Symbol	Parameter	VDD=5V±10%		VDD=3V±10%		VDD=2V*		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	0	2000	0	500	0	250	kHz
t_{SKH}	SK High Time	250	—	1000	—	2000	—	ns
t_{SKL}	SK Low Time	250	—	1000	—	2000	—	ns
t_{CSS}	CS Setup Time	50	—	200	—	200	—	ns
t_{CSH}	CS Hold Time	0	—	0	—	0	—	ns
t_{CDS}	CS Deselect Time	250	—	1000	—	1000	—	ns
t_{DIS}	DI Setup Time	100	—	400	—	400	—	ns
t_{DIH}	DI Hold Time	100	—	400	—	400	—	ns
t_{PD1}	DO Delay to '1'	—	500	—	2000	—	2000	ns
t_{PD0}	DO Delay to '0'	—	500	—	2000	—	2000	ns
t_{SV}	Status Valid Time	—	500	—	2000	—	—	ns
t_{HZ}	DO Disable Time	100	—	400	—	400	—	ns
t_{PR}	Write Cycle Time	—	5	—	5	—	—	ms

*For Read Operating Only

A.C. Test Conditions

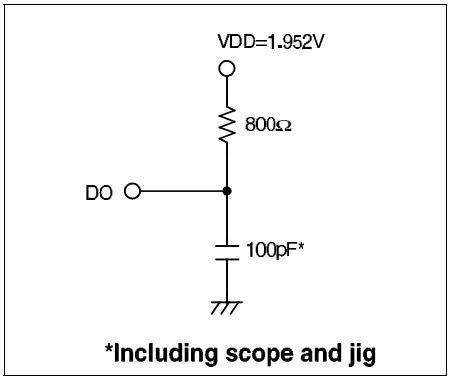
Input pluse levels: 0V to 3V

Input rise and fall time: 5ns (1V to 2V)

Input and output timing reference levels: 1.5V

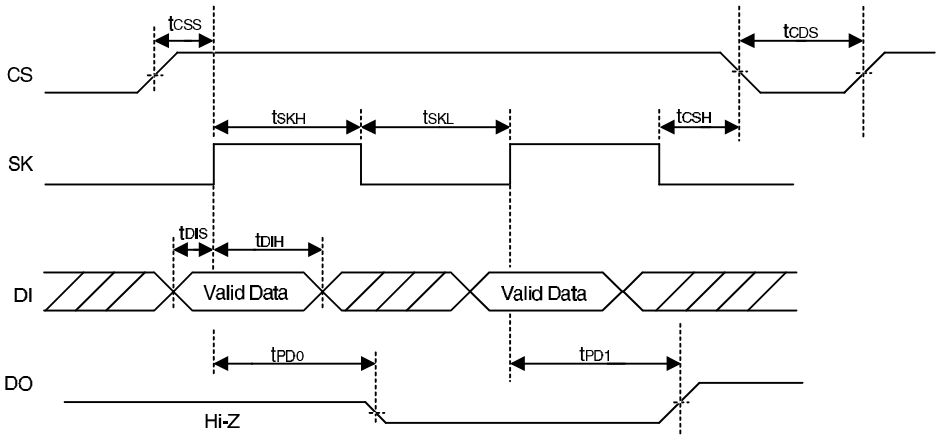
Frequency: 1MHz

Output load: See Figure right



Output Load Circuit

Timing Diagrams



Functional Description

The HT93LC46 contains 7 instructions: READ, ERASE, WRITE, EWEN, EWDS, ERAL and WRAL. These instructions are all made up of 9 bits data: 1 start bit, 2 op code bits and 6 address bits. By using the control signal CS, SK and data input signal DI, these instructions can be given to the HT93LC46 separately. These serial instruction data presented at the DI input will be written into the device at the rising edge of SK. During the READ cycle, DO pin acts as the data output and during the WRITE or ERASE cycle, DO pin indicates the BUSY/READY status. When the DO pin to be active for read data or as a BUSY/READY indicator the CS pin must be high; otherwise DO pin will be in a high-impedance state. For successful instructions, CS must be low once after the instruction is sent. After power on, the device is defautly in the EWDS state. And, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. Following are the functional descriptions and timing diagrams of all 7 instructions.

READ

The READ instruction will stream out data at a specified address on the DO pin. The data on DO pin changes during the low-to-high edge of SK signal. And the 16 bits data stream is preceded by a logical '0' dummy bit. Irrespective of the condition of the EWEN or EWDS instruction, the READ command is always valid and independent of these two instructions. After the data word has been read the internal address will be automatically incremented by 1 allowing the next consecutive data word to be read out without entering further address data. The address will wrap around with CS High until CS returns to LOW.

EWEN/EWDS

The EWEN/EWDS instruction will enable or disable the programming capabilities. At both the power on and power off state the device is automatically entered the disable mode. Before a WRITE, ERASE, WRAL or ERAL instruction is given, the programming enable instruction EWEN must be issued, otherwise the ERASE/WRITE instruction is invalid. After the EWEN instruction is issued, the programming enable condition remains until power is turned off or a EWDS instruction is given. None data can be written into the device in the programming disabled state. By so doing, the internal memory data can be protected.

ERASE

The ERASE instruction erases data at the specified addresses in the programming enable mode. After the ERASE op-code and the specified address have been issued, the data erasing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the internal erasing, so the SK clock is not required. During the internal erasing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instructions can be executed.

WRITE

The WRITE instruction writes data into the device at the specified addresses in the programming enable mode. After the WRITE op-code and the specified address and data have been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the internal writing, so the SK clock is not required. The auto-timing write cycle includes an automatic erase-before-write capability. So, it is not necessary to erase data before the WRITE instruction. During the internal writing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instructions can be executed.

ERAL

The ERAL instruction erases the entire 64x16 memory cells to logical '1' state in the programming enable mode. After the erase-all instruction set has been issued, the data erasing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the erase-all operation, so the SK clock is not required. During the internal erase-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed.

WRAL

The WRAL instruction writes data into the entire 64×16 memory cells in the programming enable mode. After the write-all instruction set has been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the write-all operation, so the SK clock is not required. During the internal write-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed.

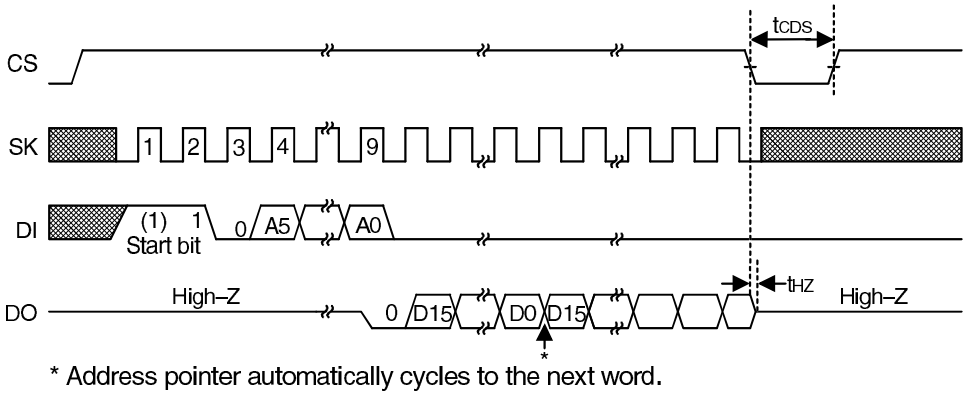
Instruction Set

Instruction	Comments	Start bit	Op Code	Address	Data
READ	Read data	1	10	A5~A0	D15~D0
ERASE	Erase data	1	11	A5~A0	—
WRITE	Write data	1	01	A5~A0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXX	—
EWDS	Erase/Write Disable	1	00	00XXXX	—
ERAL	Erase All	1	00	10XXXX	—
WRAL	Write All	1	00	01XXXX	D15~D0

Note: X stands for "don't care"

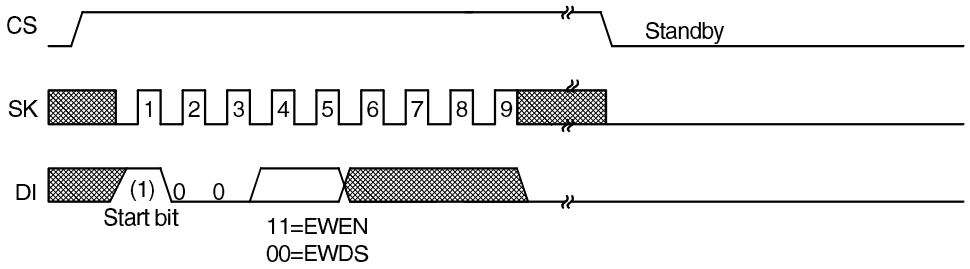
Instruction Timing

READ

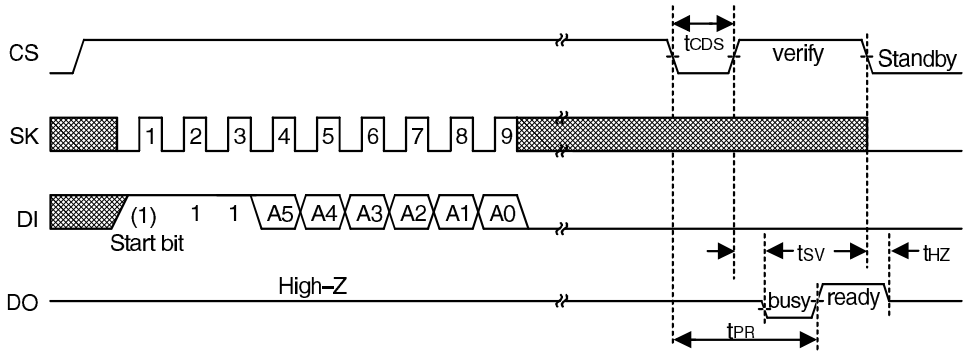


* Address pointer automatically cycles to the next word.

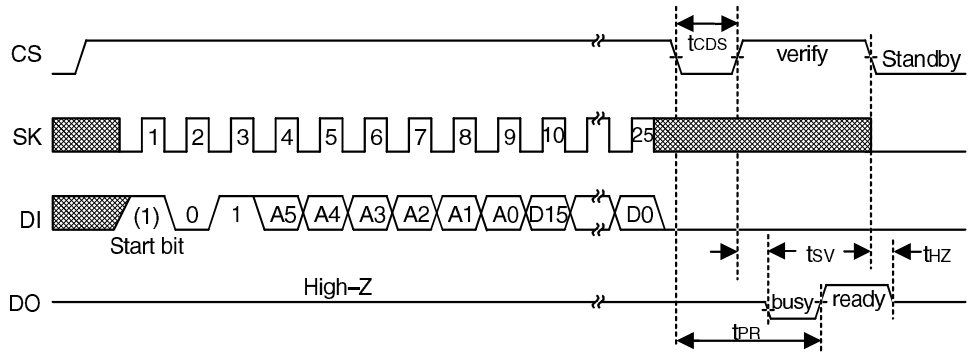
EWEN/EWDS



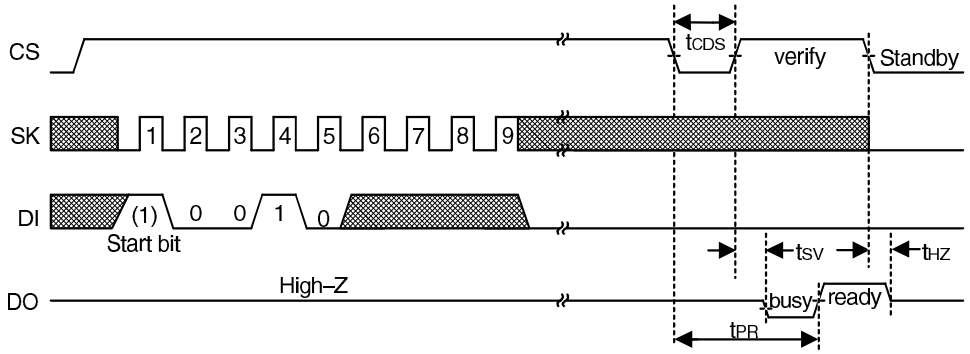
ERASE



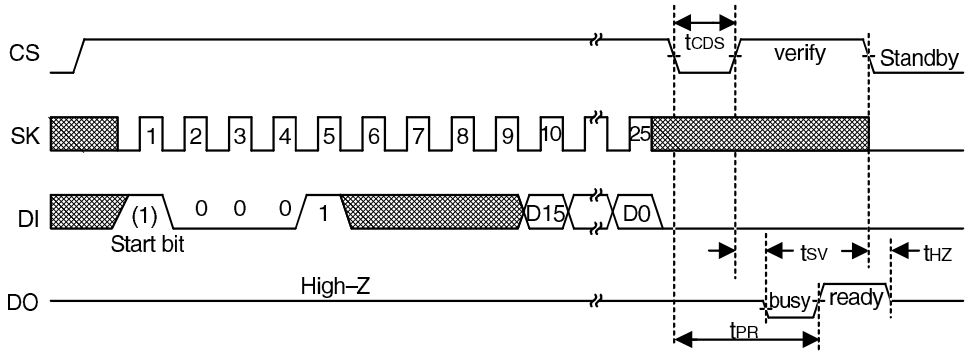
WRITE



ERAL



WRAL



Characteristic Curves