HT9200A/B
Tone (DTMF) Generators

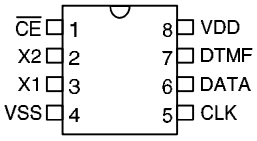
Features

- Operating voltage: 2.0V~5.5V
- Serial mode for the HT9200A
- Serial/parallel mode for the HT9200B
- Low stand-by current
- Low total harmonic distortion
- A 3.58MHz crystal or ceramic resonator

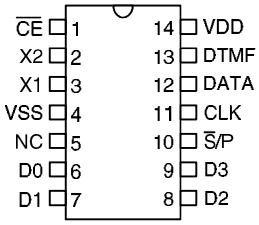
General Description

The HT9200A/B tone generators are designed for µC interfaces. They can be commanded by a µC to generate 16 dual tones and 8 single tones from the DTMF pin. The HT9200A provides a serial mode whereas the HT9200B contains a selectable serial/parallel mode interface for various applications such as security systems, home automation, remote control through telephone lines, communication systems, etc.

Pin Assignment

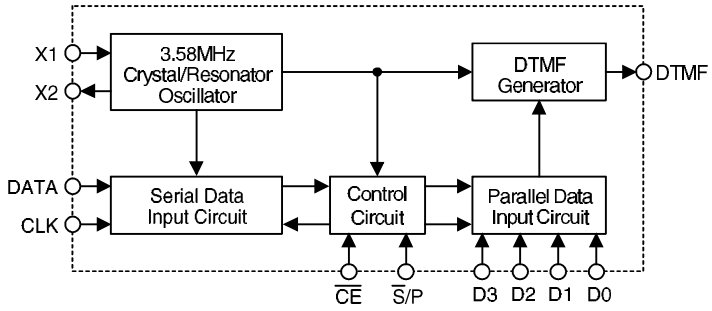


HT9200A
– 8 DIP/SOP



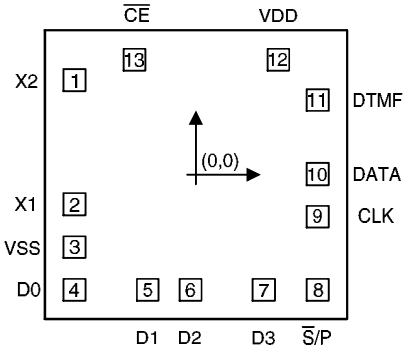
HT9200B
– 14 DIP/SOP

Block Diagram



Pad Coordinates

Unit: μm



Pad No.	X	Y	Pad No.	X	Y
1	–553.30	430.40	8	553.30	–523.50
2	–553.30	–133.50	9	553.30	–190.30
3	–553.30	–328.50	10	553.30	4.70
4	–553.30	–523.50	11	553.30	340.30
5	–220.10	–523.50	12	374.90	523.50
6	–25.10	–523.50	13	–279.30	523.50
7	308.10	–523.50			

Chip size: 1460 × 1470 $(\mu m)^2$

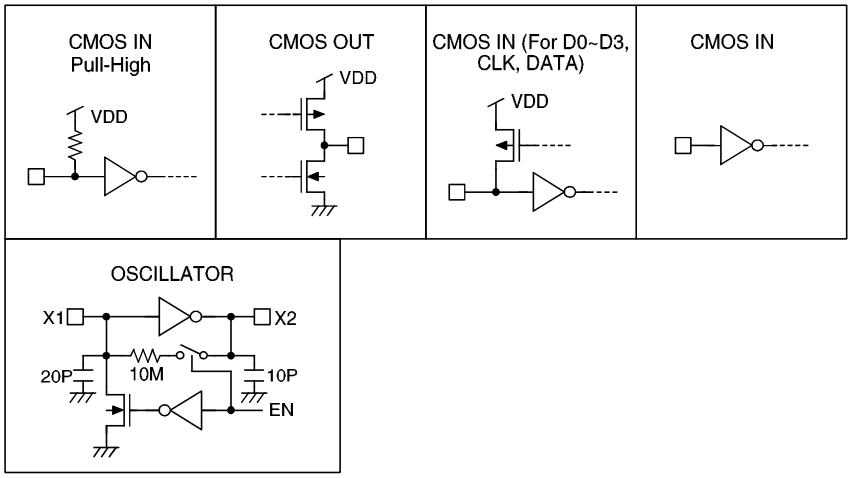
* The IC substrate should be connected to VSS in the PCB layout artwork.

Pin Description (for HT9200B)

Pin No.	Pin Name	I/O	Internal Connection	Descriptions
1	$\overline{CE}$	I	CMOS IN Pull-High	Chip enable, active low
2	X2	O	Oscillator	The system oscillator consists of an inverter, a bias resistor, and a required load capacitor on chip. The oscillator function can be implemented by connecting a standard 3.579545MHz crystal to the X1 and X2 terminals.
3	X1	I		
4	VSS	I	—	Negative power supply
5	NC	—	—	No connection
6~9	D0~D3	I	CMOS IN Pull-High or Floating	Data inputs for the parallel mode When the IC is operating in the serial mode, the data input terminals (D0~D3) are included with a pull-high resistor. When the IC is operating in the parallel mode, these pins become floating.
10	$\overline{S}$/P	I	CMOS IN	Operation mode selection input $\overline{S}$/P="H": Parallel mode $\overline{S}$/P="L": Serial mode
11	CLK	I	CMOS IN Pull-High or Floating	Data synchronous clock input for the serial mode When the IC is operating in the parallel mode, the input terminal (CLK) is included with a pull-high resistor. When the IC is operating in the serial mode, this pin becomes floating.

Pin No.	Pin Name	I/O	Internal Connection	Descriptions
12	DATA	I	CMOS IN Pull-High or Floating	Data input terminal for the serial mode When the IC is operating in the parallel mode, the input terminal (DATA) is included with a pull-high resistor. When the IC is operating in the serial mode, this pin becomes floating.
13	DTMF	O	CMOS OUT	Output terminal of the DTMF signal
14	VDD	I	—	Positive power supply, 2.0V~5.5V for normal operation

Approximate internal connection circuits



Absolute Maximum Ratings

Supply Voltage ..... –0.3V to 6V
Input Voltage..... V_{SS}–0.3 to V_{DD}+0.3V
Storage Temperature..... –50°C to 125°C
Operating Temperature..... –20°C to 75°C

Electrical Characteristics

D.C. Electrical Characteristics (Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operation Voltage	—	—	2	—	5.5	V
I_{DD}	Operation Current	2.5V	$\overline{S}/P$=V_{DD},D0~D3=V_{SS}, $\overline{CE}$=V_{SS}, No load	—	240	2500	μA
		5.0V		—	950	3000	
V_{IL}	"Low" Input Voltage	—	—	VSS	—	0.2V_{DD}	V

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{IH}	"High" Input Voltage	—	—	$0.8V_{DD}$	—	V_{DD}	V
I_{STB}	Stand-by Current	2.5V	$\overline{S}/P=V_{DD}$, $\overline{CE}=V_{DD}$, No load	—	—	1	μA
		5.0V		—	—	2	
R_P	Pull-High Resistance	2.5V	V_{OL}=0V	120	180	270	KΩ
		5.0V		45	68	100	
T_{DE}	DTMF Output Delay Time (Parallel Mode)	5V	—	—	T_{UP}+6	T_{UP}+8	ms
V_{TDC}	DTMF Output DC Level	2V~ 5.5V	DTMF Output	$0.45V_{DD}$	—	$0.75V_{DD}$	V
I_{TOL}	DTMF Sink Current	2.5V	V_{DTMF}=0.5V	–0.1	—	—	mA
V_{TAC}	DTMF Output AC Level	2.5V	Row group, R_L=5KΩ	0.12	0.15	0.18	Vr.m.s
A_{CR}	Column Pre-emphasis	2.5V	Row group=0dB	1	2	3	dB
R_L	DTMF Output Load	2.5V	THD≤–23dB	5	—	—	KΩ
THD	Tone Signal Distortion	2.5V	R_L=5KΩ	—	–30	–23	dB
F_{CLK}	Clock Input Rate (Serial Mode)	—	—	—	100	500	KHz
T_{UP}	Oscillator Starting Time (When $\overline{CE}$ is low)	5.0V	The time from $\overline{CE}$ falling edge to normal oscillator operation	—	—	10	ms
F_{OSC}	System Frequency	—	Crystal=3.5795MHz	3.5759	3.5795	3.5831	MHz

Functional Description

The HT9200A/B are DTMF generators for μC interfaces. They are controlled by a μC in the serial mode or the parallel mode (for the HT9200B only).

Serial mode (HT9200A/B)

The HT9200A/B employ a data input, a 5 bit code, and a synchronous clock to transmit a DTMF signal. Every digit of a phone number to be transmitted is selected by a series of inputs which consist of 5 bit data. Of the 5 bits, the D0(LSB) is the first received bit. The HT9200A/B will latch data on the falling edge of the clock (CLK pin). The relationship between the digital codes and the tone output frequency is shown in Table 1. As for the control timing diagram, refer to Figure 1.

When the system is operating in the serial mode a pull-high resistor is put to D0~D3 (used in the parallel mode) on the input terminal.

For the HT9200B, the $\overline{S}$/P pin has to be connected low for operating in the serial mode.

Table 1: Digits vs. input data vs. tone output frequency (serial mode)

Digit	D4	D3	D2	D1	D0	Tone Output Frequency (Hz)
1	0	0	0	0	1	697+1209
2	0	0	0	1	0	697+1336
3	0	0	0	1	1	697+1477
4	0	0	1	0	0	770+1209
5	0	0	1	0	1	770+1336
6	0	0	1	1	0	770+1477
7	0	0	1	1	1	852+1209
8	0	1	0	0	0	852+1336
9	0	1	0	0	1	852+1477
0	0	1	0	1	0	941+1336
*	0	1	0	1	1	941+1209
#	0	1	1	0	0	941+1477
A	0	1	1	0	1	697+1633
B	0	1	1	1	0	770+1633
C	0	1	1	1	1	852+1633
D	0	0	0	0	0	941+1633
—	1	0	0	0	0	697
—	1	0	0	0	1	770
—	1	0	0	1	0	852
—	1	0	0	1	1	941
—	1	0	1	0	0	1209
—	1	0	1	0	1	1336
—	1	0	1	1	0	1477
—	1	0	1	1	1	1633
DTMF OFF	1	1	1	1	1	—

*Note: (1) The codes not listed in Table 1 are not used.
(2) The D4 is MSB.

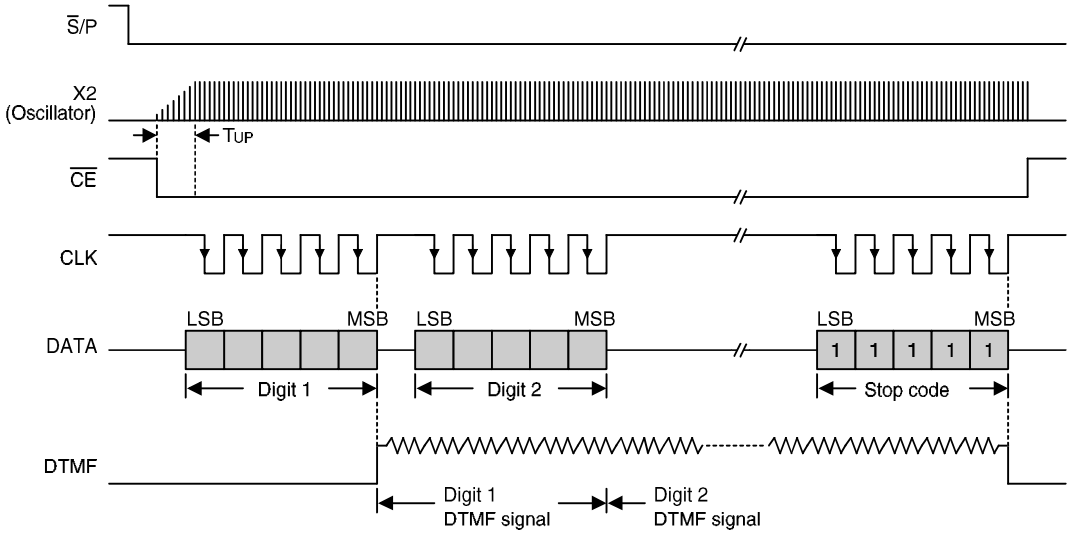


Figure 1

Parallel mode (HT9200B)

The HT9200B provides four data inputs D0~D3 to generate their corresponding DTMF signals. The S/P has to be connected high to select the parallel operation mode. Then the input data codes should be decided. Finally, the CE is connected low to transmit the DTMF signal from the DTMF pin.

The T_{DE} time (about 6ms) will be delayed from the CE falling edge to the DTMF signal output.

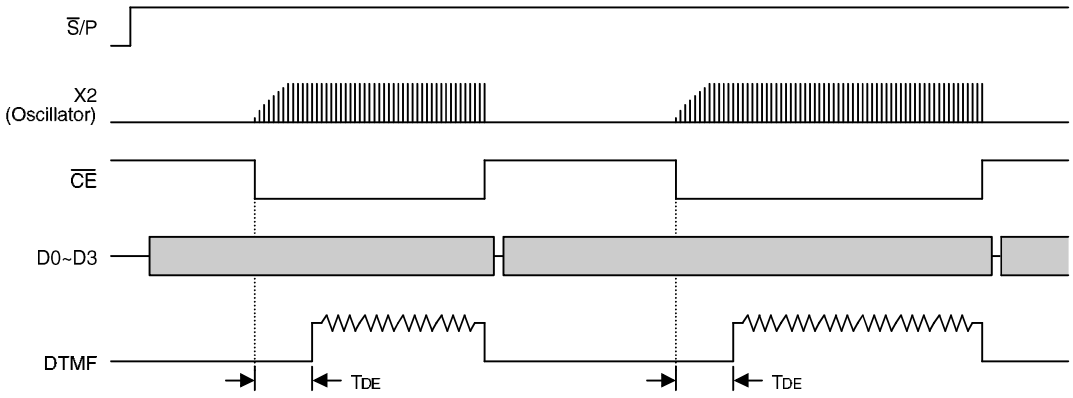
The relationship between the digital codes and the tone output frequency is illustrated in Table 2. As for the control timing diagram, see Figure 2.

When the system is operating in the parallel mode, D0~D3 are all in the floating state. Thus, these data input pins should not float.

Table 2: Digits vs. input data vs. tone output frequency (parallel mode)

Digit	D3	D2	D1	D0	Tone Output Frequency (Hz)
1	0	0	0	1	697+1209
2	0	0	1	0	697+1336
3	0	0	1	1	697+1477
4	0	1	0	0	770+1209
5	0	1	0	1	770+1336
6	0	1	1	0	770+1477
7	0	1	1	1	852+1209
8	1	0	0	0	852+1336
9	1	0	0	1	852+1477

Digit	D3	D2	D1	D0	Tone Output Frequency (Hz)
0	1	0	1	0	941+1336
*	1	0	1	1	941+1209
#	1	1	0	0	941+1477
A	1	1	0	1	697+1633
B	1	1	1	0	770+1633
C	1	1	1	1	852+1633
D	0	0	0	0	941+1633



* Note: The data (D0~D3) should be ready before the $\overline{CE}$ becomes low.

Figure 2

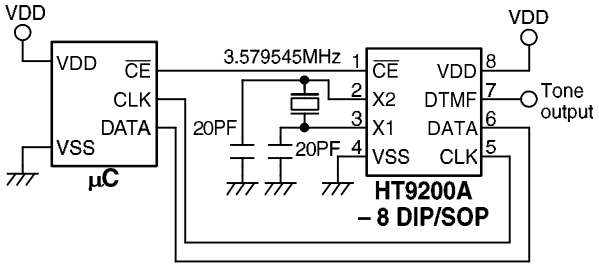
Tone Frequency

Output Frequency (Hz)		%Error
Specified	Actual	
697	699	+0.29%
770	766	–0.52%
852	847	–0.59%
941	948	+0.74%
1209	1215	+0.50%
1336	1332	–0.30%
1477	1472	–0.34%

% Error does not contain the crystal frequency drift.

Application Circuits

Serial mode



Serial/Parallel mode