HT1380
Serial Timekeeper Chip

Features

- Operating Voltage: 2.0V~5.5V
- Maximum input serial CLK: 500KHz at VDD=2V, 2MHz at VDD=5V
- Operating current: less than 300nA at 2V, less than 1μA at 5V
- TTL compatible:
  - VIH: 2.0V~VDD+0.3V at VDD=5V
  - VIL: –0.3V~+0.8V at VDD=5V
- Two data transmission modes: Single-byte, or Multiple-byte (Burst mode)
- Serial I/O transmission
- All registers store BCD format

Applications

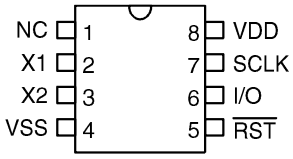
- Microcomputer serial clock
- Clock and Calendar

General Description

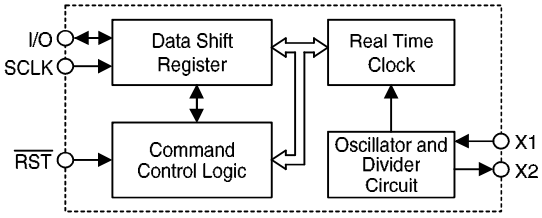
The HT1380 is a serial timekeeper IC which provides seconds, minutes, hours, day, date, month and year information. The number of days in each month and leap years are automatically adjusted. Also, the HT1380 is designed for low power consumption and can operate in one of two formats: a 12-hour mode with an AM/PM indicator, or a 24-hour mode.

The HT1380 has several registers to store the corresponding information. An 32.768Hz off-chip crystal is required to provide the correct timing. In order to minimize the pin number, the HT1380 uses a serial I/O transmission method to interface with a microprocessor. Only three wires are required. (1)$\overline{\text{RST}}$, (2)SCLK and (3)I/O. Data can be delivered one byte at a time or in a burst of up to 8 bytes.

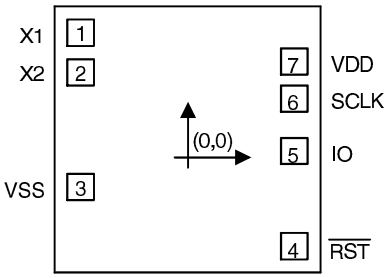
Pin Assignment



Blcok Diagram



Pad Assignment & position



Chip Size: 2480 x 2390 $(um)^2$

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1060.5	1000	5	1050.6	54.15
2	–1060.5	683.13	6	1050.8	472.16
3	–1060.5	–236.14	7	1050.4	770.21
4	1050.62	–710			

Pin Description

Pad No.	Pin Name	I/O	Description
1	NC	—	Not connected
2,3	X1,X2	I	Off-chip 32.768KHz crytal
4	VSS	I	Ground pin
5	$\overline{RST}$	I	The reset pin of serial transmission
6	I/O	I/O	The data input/output pin of serial transmission
7	SCLK	I	The serial clock pulses pin of serial transmission
8	VDD	I	Power supply pin

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature..... –50°C to 125°C
Operating Temperature ..... 0°C to 70°C

D.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operation voltage	—	—	2	—	5.5	V
I_{STB}	Stand-by current	2V	—	—	—	100	nA
		5V		—	—	100	nA
I_{DD}	Operation current	2V	No load	—	—	0.3	μA
		5V		—	—	1.0	μA
I_{OH}	Source current	2V	V_{OH}=1.8V	–0.2	–0.4	—	mA
		5V	V_{OH}=4.5V	–0.5	–1.0	—	mA
I_{OL}	Sink current	2V	V_{OL}=0.2V	0.7	1.5	—	mA
		5V	V_{OL}=0.5V	2.0	4.0	—	mA
V_{IH}	"H" input voltage	5V	—	2	—	—	V
V_{IL}	"L" input voltage	5V	—	—	—	0.8	V
F_{OSC}	System frequency	5V	32.768KHz XTAL	—	32.768	—	KHz
F_{SCLK}	Serial clock	2V	—	—	—	0.5	MHz
		5V		—	—	2	MHz

* I_{STB} is specified with SCLK, I/O, $\overline{RST}$ open. The clock halt bit must be set to logic one (oscillator disabled).

A.C. Characteristics

(Ta=25°C)

Symbol	Parameter	VDD	Min.	Max.	Unit
t_{DC}	Data to clock setup	2V	200	—	ns
		5V	50	—	
t_{CDH}	Clock to data hold	2V	280	—	ns
		5V	70	—	
t_{CDD}	Clock to data delay	2V	—	800	ns
		5V	—	200	
t_{CL}	Clock low time	2V	1000	—	ns
		5V	250	—	
t_{CH}	Clock high time	2V	1000	—	ns
		5V	250	—	
f_{CLK}	Clock frequency	2V	—	0.5	MHz
		5V	D.C.	2.0	
t_R t_F	Clock rise & fall time	2V	—	2000	ns
		5V	—	500	
t_{CC}	Reset to clock setup	2V	4	—	us
		5V	1	—	
t_{CCH}	Clock to reset hold	2V	240	—	ns
		5V	60	—	
t_{CWH}	Reset inactive time	2V	4	—	us
		5V	1	—	
t_{CDZ}	Reset to I/O high Z	2V	—	280	ns
		5V	—	70	

Function Description

The HT1380 mainly contains the following elements: a data shift register array to store the clock/calendar data, command control logic, oscillator circuit and read timer clock. Two mode are available to transfer the data from and to the HT1380. The two mode are single-byte mode and multiple-byte.

To initiate any transfer of data, $\overline{RST}$ is taken high and an eight bit command byte is first loaded into the control logic to provide the register address and command information. Following the command word, the clock/calendar data is transferred to or from the corresponding register serially. The $\overline{RST}$ pin must be taken low again after the transfer operation is complete. All data is inputted on the rising edge of SCLK and outputs on the falling edge of SCLK. In total,16 clocks pulses are needed for byte mode and 72 of those for burst mode. Both input and output data starts with bit 0.

The HT1380 also contains two additional bits, the clock halt bit (CH) and the write protect bit (WP). These bits control the operation of the oscillator and to control if data can be written to the register array. These two bits should first be specified in order to read from and write to the register array properly.

Command byte

For each data transfer, a command byte is initiated to specify which register is accessed. This is to decide to be whether a read, write, or test cycle is operated and whether a byte or burst mode transfer is to occur. The command byte is shown as follows:

7	6	5	4	3	2	1	0
1	0	0	A3	A2	A1	A0	R/$\overline{W}$

A0~A2 : The address of register.
A3 : 1 for test mode, 0 for normal mode.
R/W : 1 for read cycle, 0 for write cycle.

The LSB set to logic zero(one), represents a write(read) cycle is to take place. Bits one through three specify the designated registers to be accessed. If the command byte is 1001xxx1, the HT1380 is configured in Test mode. The Test mode is used by HOLTEK only for testing purposes. If used generally, unpredictable conditions may occur.

The following table shows the register address and its data format:

Register address A2~A0	Function	Command Address (HEX)	Write=W Read=R	Range Data (BCD)	Register Definition							
					7	6	5	4	3	2	1	0
0	Seconds	80 81	W R	00~59	CH	10 SEC			SEC			
1	Minutes	82 83	W R	00~59	0	10 MIN			MIN			
2	12HRS 24HRS	84 85	W R	01~12 00~23	12\ 24	0 0	AP 10	HR HR	HOUR			
3	Date	86 87	W R	01~31	0	0	10 DATE		DATE			
4	Month	88 89	W R	01~12	0	0	0	10M	MONTH			
5	Day	8A 8B	W R	01~07	0	0	0	0	DAY			
6	Year	8C 8D	W R	00~99	10 YEAR				YEAR			
7	Write Protect	8E 8F	W R	00~80	WP	ALWAYS ZERO						

CH: Clock Halt bit.
CH=0 oscillator enabled.
CH=1 oscillator disabled.

WP: Write protect bit.
WP=0 register data can be written in.
WP=1 register data can not be written in.

Bit 7 of Reg2: 12/24 mode flag.
bit 7=1, 12-hour mode.
bit 7=0, 24-hour mode.

Bit 5 of Reg2: AM/PM mode defined.
AP=1 PM mode.
AP=0 AM mode.

Clock halt bit

Bit 7 of the seconds register is defined as the clock halt bit (CH). When this bit is set to logic one, the clock oscillator is stopped and the HT1380 is placed into a low-power stand-by mode. When this bit is written to logic zero, the clock will start.

Write protect register

Data can be written into the designated register only if the write protect bit (WP), the MSB of write protect register is set to logic zero. The write protect register can be accessed using the command $8E or $8F. The write protect bit cannot be written to in burst mode.

Reset and Clock control

The $\overline{RST}$ pin is used to enable the HT1380. When the $\overline{RST}$ pin is taken high, the built-in control logic is turned on and the address/command sequence can access the corresponding shift register. The $\overline{RST}$ pin is also used to terminate either single byte or multiple byte data transfer. The user should take the $\overline{RST}$ pin low again after every data transfer operation is completed. The input of SCLK is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of SCLK. The data bits are outputted on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ input is low and the I/O pin goes to a high impedance state.

Burst mode

When the command byte is $BE (or $BF), the HT1380 is configured in burst mode. In this mode the eight clock/calendar registers can be consecutively written (or read) starting with bit 0 of register address 0.

Data in and Data out

For writing a data byte in the HT1380, the user should first input the "write command byte" and follow with the coresponding data byte on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored. Data is inputted starting with bit 0.

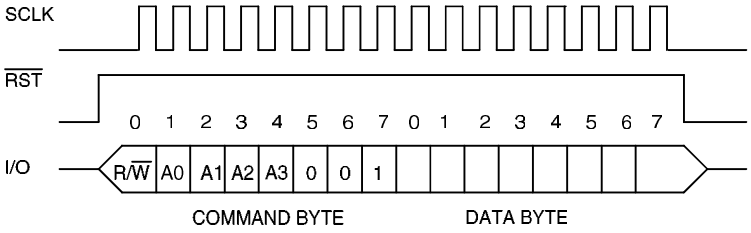
For reading a data byte from the HT1380, a "read command byte" should be first input. The data bit is outputted on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted on the first falling edge after the last bit of the "read command byte" is written. Additional SCLK cycles retransmit the data bytes as long as $\overline{RST}$ remains high level. Data is outputted starting with bit 0.

Crystal selection

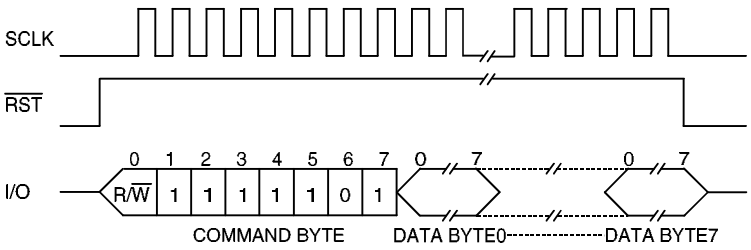
A 32.768Khz crystal can be directly connected to the HT1380 via pin 2 and 3 (X1, X2). In order to obtain the correct frequency, a crystal with 8pF load capacitance, should be selected.

The following diagram shows the single and burst mode transfer:

Single Byte Transfer

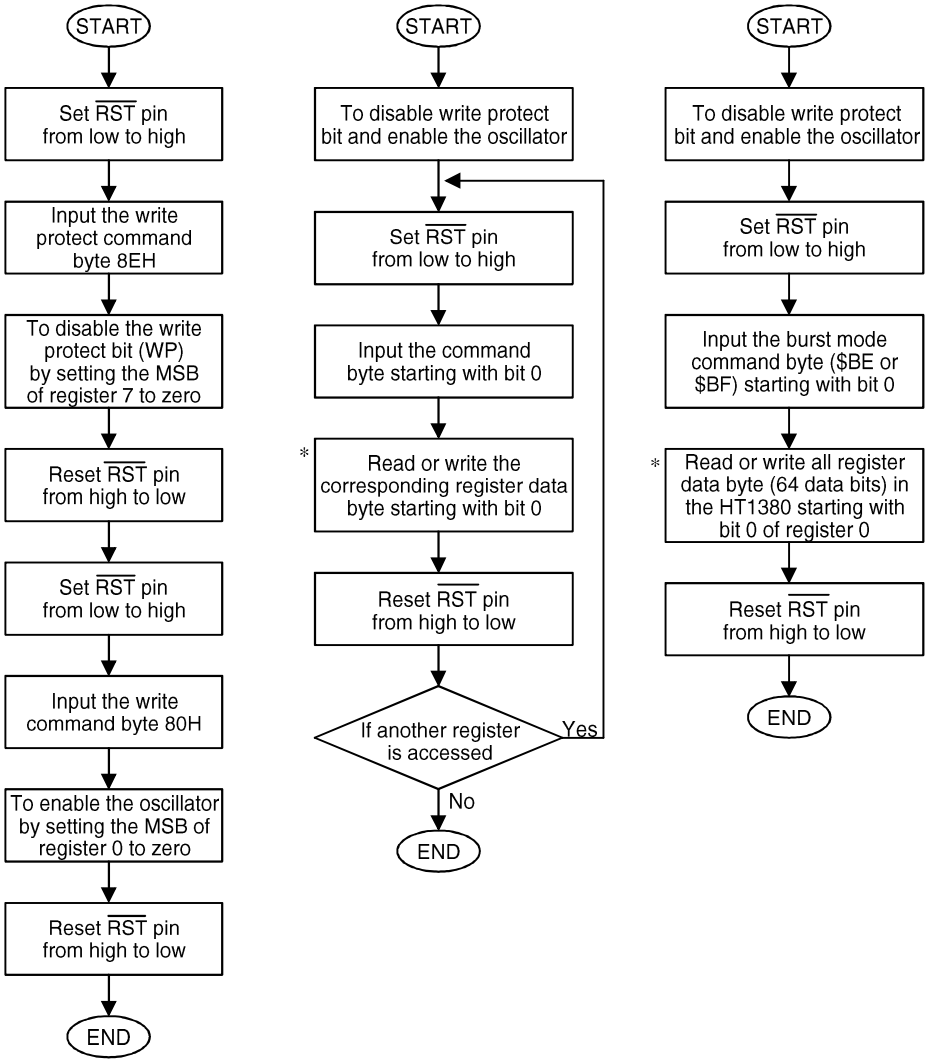


Burst Mode Transfer



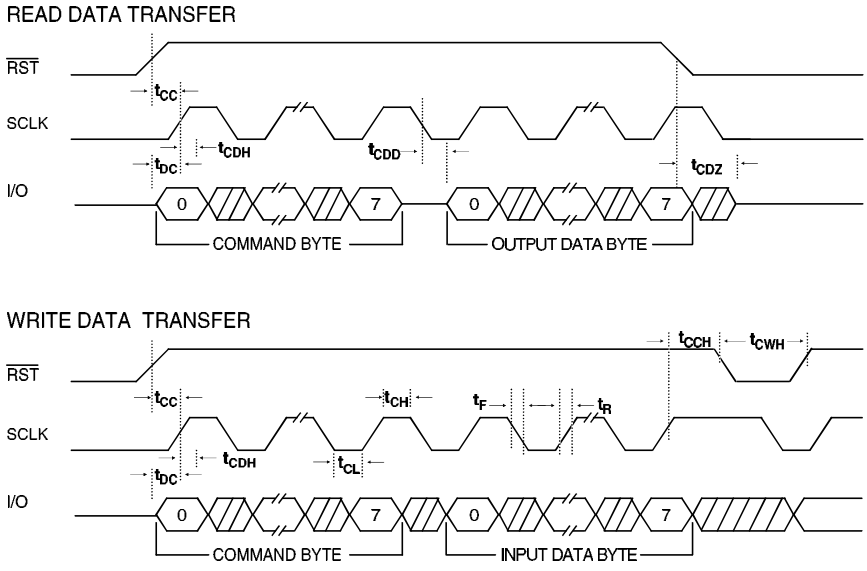
Flow Chart

- To disable write protect (WP=0) bit and enable the oscillator (CH=0)
- Single byte data tranfer
- Burst mode data transfer



* For reading data byte from HT1380 register, the first data bit to be transmitted at the first falling edge after the last bit of the command byte is written.

Timing Diagram



Application Diagram